Amendment to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A storage container structure comprising:

a single layer substrate including a doped semiconductor structure;

a single layer of insulating material disposed over and in contact with said substrate, said insulating material of sufficient depth to include a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region comprising a doped topographic core, said patterning stop region disposed over and in contact with said substrate such that a substantial entirety of the width of said container region is defined by an upper surface of said patterning stop region;

a charge storage lamina formed over an interior surface of said container region, said charge storage lamina comprising a first conductive film with at least a portion thereof in contact with said patterning stop region, a second conductive film defining a first surface thereon, and an insulating film disposed intermediate said first and second conductive films;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by said first surface of said second conductive film; and

an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

2. (Currently Amended) A storage container structure comprising:

a single layer substrate including a doped semiconductor structure;

a patterning stop region comprising a doped topographic core, said patterning stop region disposed over and in contact with said substrate such that a substantial entirety of the width of said container region is defined by an upper surface of said patterning stop region;

a single layer of insulating material disposed over and in contact with said substrate;

a container region formed within said insulating material, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall, wherein all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina formed over an interior surface of said container region, said charge storage lamina comprising a first conductive film with at least a portion thereof in contact with said patterning stop region, a second conductive film defining a first surface thereon, and an insulating film disposed intermediate said first and second conductive films;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

3. (Currently Amended) A storage container structure comprising:

a single layer substrate including a doped semiconductor structure, said substrate including a generally planar upper surface;

a single layer of insulating material disposed over and in contact with said generally planar upper surface of said substrate, said insulating material including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region comprising a doped topographic core, said patterning stop region including:

a lower surface disposed over and in contact with said generally planar upper surface of said substrate; and

an upper surface configured such that the lowermost extension of said container bottom wall does not project substantially below said upper surface of said patterning stop region, said upper surface configured such that a substantial entirety of said container cross section is defined by said upper surface;

a charge storage lamina formed over an interior surface of said container region, said charge storage lamina comprising a first conductive film with at least a portion thereof in contact with said patterning stop region, a second conductive film defining a first surface thereon, and an insulating film disposed intermediate said first and second conductive films;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

4. (Currently Amended) A storage container structure comprising:

a single layer substrate including a doped semiconductor structure, said substrate including a generally planar upper surface;

an insulating material disposed over and in contact with said generally planar upper surface of said substrate, said insulating material including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region <u>comprising a doped topographic core, said patterning stop region</u> including:

a lower surface in contact with said generally planar upper surface of said substrate; and

an upper surface configured to define a substantial entirety of said container cross section;

a charge storage lamina over an interior surface of said container region, said charge storage lamina comprising a first conductive film with at least a portion thereof in contact with said patterning stop region, a second conductive film defining a first surface thereon, and an insulating film disposed intermediate said first and second conductive films;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

5. (Original) A storage container structure according to claim 4, wherein said upper surface of said patterning stop region is configured such that all of said container bottom wall is defined by said upper surface of said patterning stop region.

6. (Withdrawn) A memory device comprising:

a storage container structure comprising:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side

walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region; and

a bit line terminal coupled to said charge storage lamina through a switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command.

7. (Withdrawn) A computer system comprising:

a storage container structure including:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region;

a bit line terminal coupled to said charge storage lamina through a switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command; and

a microprocessor in communication with a plurality of said charge storage structures via respective ones of a plurality of said bit line terminals.

8. (Withdrawn) A memory device comprising:

a storage container structure including:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a transistor switching structure;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region, said patterning stop region forming part of said transistor switching structure;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.; and

a bit line terminal coupled to said charge storage lamina through said switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command.